REMARKS

Claims 1, 3, 5-9, 11, 13, 15-18 and 20 are all the claims pending in the application. Claims 1 and 7 are amended with the features at least found on page 3, lines 22-24 of the specification.

Claim rejections under 35 U.S.C. § 112, first paragraph

Claim 5 is rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement. The Examiner asserts on page 3 of the Office Action that "in the case of vector quantization, the Applicant has gone into great detail to describe how parallel processors in a DSP are configured to achieve their invention, but in the case of the CELP processing there is no mention of how the DSP may be configured to achieve this aspect of the invention." Moreover, the Examiner contends that "since it only generically mentions parallel processing in passing, the disclosure with respect to claim 5 is insufficient. The cited portions of the Applicant's disclosure are not convincing because they lack the aforementioned description and merely replicate the generic statement that is already featured in claim 5." Applicants traverse the rejection for at least the following reasons.

MPEP § 2164.01 states that:

> Any analysis of whether a particular claim is supported by the disclosure in an application requires a determination of whether that disclosure, when filed, contained sufficient information regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention. The standard for determining whether the specification meets the enablement requirement was cast in the Supreme Court decision of *Mineral Separation v. Hyde,* 242 U.S.

> 261, 270 (1916) which postured the question: is the experimentation needed to practice the invention undue or unreasonable? That standard is still the one to be applied. *In re Wands*, 858 F.2d 731, 737, 8 USPQ2d 1400, 1404 (Fed. Cir. 1988). Accordingly, even though the statute does not use the term "undue experimentation," it has been interpreted to require that the claimed invention be enabled so that any person skilled in the art can make and use the invention without undue experimentation. *In re Wands*, 858 F.2d at 737, 8 USPQ2d at 1404 (Fed. Cir. 1988).

Regarding the Examiner assertion that the cited portion of the Applicant's disclosure only generically mentions parallel processing in passing, Applicants respectfully note that at page 9, last line to page 10, line 5, the specification describes that:

> An additional reduction of execution time is achieved by generating/evaluating elements of matrices representing a transfer function of at least one filter of said synthesis section SYN, and/or elements of auto-correlation matrices used within said CELP-algorithm, in parallel. A significant decrease of execution time can especially be achieved by parallel processing of the elements of said auto-correlation matrices because these matrices must be cyclically re-calculated.

Furthermore, the specification at page 10, lines 6-10 describes that:

> The signal values of said speech signal s and of said elements of said auto-correlation matrices are represented by 16 bit data words, and since a 64 bit memory read instruction is provided by the DSP, four signal values located in a memory of said DSP <u>are accessed simultaneously</u> which ensures that even in case of simultaneous evaluation of a plurality of signal values input data is always available.

Accordingly, the specification describes how the auto-correlation matrices are represented and how they are accessed and processed (i.e., accessed simultaneously). Therefore,

Applicants respectfully submit that the claimed feature is not merely mentioned generically as contended by the Examiner. To the contrary, the specification does provide sufficient information so that a person of ordinary skill in the art can readily make and use the invention without undue experimentation, and therefore claim 5 complies with the enablement requirement.

Further, Applicants note that it would be practically impossible to describe in the claim or even in the specification every possible way of using the parallel processing, and then to explain how the DSP would be configured to achieve the parallel processing for every possible way. The patent laws and rules do not require such an exhaustive recitation. It is sufficient that the description explains the invention to the level of the artisan of ordinary skill, and that the claim defines the boundaries of protection sought. A person of ordinary skill would readily understand that an additional reduction of execution time is achieved by generating/evaluating elements of matrices representing a transfer function of at least one filter of said synthesis section SYN, and/or elements of auto-correlation matrices used within said CELP-algorithm, in parallel.

In view of the above, Applicants respectfully request the Examiner to withdraw this rejection of claim 5.

Claims rejection under 35 U.S.C. § 103

Claims 1, 3, 5-9, 11, 13 and 15-18 and 20 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Kwan et al. ("Implementation of DSP-RAM: An architecture for parallel Digital Signal Processing in Memory," 2001) in view of Davidson et al. (U.S. Patent:

4,868,867; hereinafter "Davidson"). Applicants traverse the rejection for at least the following reasons.

Claim 1 recites *inter alia*, "the evaluating the index comprises comparing the index of each optimal group code vector with indices of other optimal group code vectors". Applicants respectfully submit that Kwan and Davidson do not teach or suggest this claimed feature. On page 7 of the Office Action, the Examiner asserts that "when Kwan performs evaluation of an optimal code vector, the process comprises analysis at each code vector position in a codebook, and thus, analysis of each corresponding vector index. (pages 344-345). In this way, Kwan does teach evaluating indexes in a codebook."

However, Applicants respectfully submit that even if, *assuming arguendo*, the code vector position in a code book are analyzed, this does not teach or suggest comparing the index of each optimal group code vector with indices of other optimal group code vectors. That is, according to the claimed invention, indices are being compared with each other. This feature is not disclosed in Kwan and is also not obvious.

In addition, since Kwan discloses analyzing the code vector already in sequence within the processor on pages 344-345, as acknowledged by the Examiner, there would be no rationale for providing the feature of comparing the indices to ensure conformity with the linear processes.

Davidson does not disclose these features missing in Kwan.

In view of the above, Applicants submit that claim 1 is allowable over the cited references.

Claim 7

Applicant respectfully submits that claim 7 recites subject matter analogous to claim 1, and therefore is allowable for at least the analogous reasons claim 1 is allowable.

Claims 3, 5-6, 8, 9, 11-18 and 20

Applicant submits that claims 3, 5-6, 8, 9, 11-18 and 20 depend from either claim 1 or 7, and therefore are allowable at least by virtue of their dependency.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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